CLAIM AMENDMENTS

1. (Currently Amended) A semiconductor device comprising an N channel metal oxide semiconductor (MOS) transistor, the N channel MOS transistor including:

a P type semiconductor substrate;

~~an~~ first and second N type epitaxial ~~region formed~~ regions on the P type semiconductor substrate;

a first P type buried layer isolating the N first and second type epitaxial ~~region~~ regions from ~~another N type epitaxial region~~ each other;

an N well ~~formed~~ in the first N type epitaxial region;

a drain region ~~formed~~ in the N well;

a P well surrounding ~~side faces~~ sides of the N well ~~so as to be separated from~~ and isolating the N well;

a source region ~~formed~~ in the P well;

a gate ~~formed~~ on ~~each~~ upper layer ~~portion~~ portions of each of the drain region and the source region;

a second P type buried layer ~~formed below~~ between the N well and the P well ~~so as to be joined~~ and the P type semiconductor substrate, contiguous to the P well and ~~to be separated from~~ not in contact with the P type semiconductor substrate and the first P type buried layer; ~~and~~

an N type buried layer ~~formed so as to be joined~~ contiguous to the second P type buried layer and the P type semiconductor substrate and ~~to be separated from~~ not in contact with the P well, the N well, and the first P type buried layer~~,~~; and

~~wherein~~ a first electrode electrically connected to the N type epitaxial region, a second electrode electrically connected to the P type semiconductor substrate, and a third electrode electrically connected to the first P type buried layer ~~are~~, the first, second, and third electrodes being connected to ground potential.

2. (Currently Amended) The semiconductor device according to claim 1, ~~wherein~~ including a connection ~~is established~~ between the first electrode and the ground potential ~~so as to be able to apply~~ so a power supply potential can be supplied to the first N type epitaxial region.

3. (Currently Amended) The semiconductor device according to claim 1, wherein the source region is ~~formed in~~ a first N type semiconductor region, and including

a fourth electrode electrically connected to the source region ~~is joined to~~ and contacting the first N type semiconductor region, and

a first P type semiconductor region surrounding the first N type semiconductor region and ~~is separated~~ spaced from the P well.

4. (Currently Amended) The semiconductor device according to claim 1, wherein the drain region is ~~formed in~~ a second N type semiconductor region.

5. (Currently Amended) The semiconductor device according to claim 1, wherein the first electrode is ~~joined~~ connected to a third N type semiconductor region ~~formed~~ in the first N type epitaxial region and is ~~separated from~~ not in contact with the N type epitaxial region.

6. (Currently Amended) The semiconductor device according to claim 1, wherein the second electrode is ~~joined~~ connected to a second P type semiconductor region ~~formed~~ in the first P type buried layer and is ~~separated from~~ not in contact with the first P type buried layer.

7. (Currently Amended) The semiconductor device according to claim 1, wherein the semiconductor device is a switching element ~~forming~~ of an inverter ~~as~~ of a motor driver ~~includes the N channel MOS transistor~~.